Tulsiramji Gaikwad-Patil College of Engineering and Technology
Wardha Road, Nagpur-441108
NAAC Accredited (A+ Grade) & NBA Accredited
An Autonomous Institute affiliated to RTMNU Nagpur

Third Year (Semester V) B.Tech. Electronics & Communication Engineering

BEC33525: System Design Through Verilog (Honor Subject)

Teaching Scheme		Examination Scheme	
Lectures	3 Hrs./week	**CT-1**	15 Marks
Tutorial	0 Hrs./week	**CT-2**	15 Marks
Total Credit	3	**TA**	10 Marks
Duration of ESE:03Hrs.		**ESE**	60 Marks
		Total	100 Marks

Course Outcomes (CO)

Students will be able to

CO1: Apply Verilog HDL for digital system modeling
CO2: Design combinational and sequential circuits using HDL
CO3: Develop FSM-based controllers and RTL systems
CO4: Implement and verify digital systems using testbenches
CO5: Analyze and optimize system-level designs using FPGA tools

Course Contents

Unit I	**Introduction to System Design & Verilog HDL:** Digital system design concepts and design methodology, Introduction to Hardware Description Languages (HDL), Verilog HDL overview and applications, Verilog structure: modules, ports, data types, operators, Gate level modeling, Dataflow modeling, Behavioral modeling, Simulation and synthesis concepts, Design flow using Verilog
Unit II	**Combinational Logic Design using Verilog:** Boolean algebra and logic gates implementation, Combinational circuit design, Verilog coding for combinational circuits, Design hierarchy and modular design, Timing concepts and delays, Verification of combinational circuits, Introduction to testbenches
Unit III	**Sequential System Design:** Sequential circuits fundamentals, Flip-flops, registers, counters, Timing issues: setup time, hold time, clocking, Finite State Machines (FSM), Verilog modeling of sequential circuits, design concepts, Simulation and debugging
Unit IV	**System-Level Design & Memory Concepts:** Memory elements, RAM, ROM, FIFO, Memory modeling in Verilog, Processor basics and Datapath design Interfacing of I/O devices and controllers, Bus structures and communication Introduction to FPGA and PLDs, System integration using Verilog
Unit V	**Advanced Topics & Applications:** Testbench design and verification techniques Design for testability (DFT), Fault simulation and debugging, Optimization techniques in digital design, Introduction to System Verilog (basic concepts), FPGA design flow and tools, Case studies: ALU design, UART / communication system, Simple processor design

Text Books

T.1	Samir Palnitkar – *Verilog HDL: A Guide to Digital Design and Synthesis*, Pearson
T.2	Peter J. Ashenden – *Digital Design: An Embedded Systems Approach Using Verilog*, Elsevier

Reference Books

R.1	Stephen Brown & Zvonko Vranesic – *Fundamentals of Digital Logic with Verilog Design*
R.2	Charles Roth – *Digital System Design Using VHDL/Verilog*

Useful Links

L.1	https://www.youtube.com/watch?v=1gdfuKVOUgQ
L.2	https://www.youtube.com/watch?v=bSuACAU025o&list=PLeIwGZPgtiz7adWh4SiHJnfPLbDvGdKk6