



TULSIRAMJI GAIKWAD-PATIL COLLEGE OF ENGINEERING & TECHNOLOGY

Wardha Road, Nagpur - 441108
Accredited with NAAC A+ Grade & NBA Accredited (EE, ME, CE & ECE)
Approved by AICTE, New Delhi, Govt. of Maharashtra
(An Autonomous Institution Affiliated to Rashtrasant Tukadoji Maharaj Nagpur University, Nagpur)



Department of Electronics and Communication Engineering

Program: B. Tech Electronics and Communication Engineering

Semester-IV **BEC32425: Hardware Modeling Using Verilog-Honour**

Teaching Scheme		Examination Scheme (Th)		Examination Scheme (P)	
Theory (Th)	3 Hrs./week	CT-I	15 Marks	-	-
Practical (P)	-	CT-II	15 Marks	-	-
Total Credits	3 (Th) = 3	CA	10 Marks	-	-
Duration of ESE: 3 Hrs.		ESE	60 Marks	-	-
		Total Marks	100 Marks	-	-

Pre-Requisites:

Course Objectives:

1	To introduce the fundamental concepts, syntax, design levels, and core language constructs of Verilog HDL for hardware description.
2	To train students in modeling digital circuits using structural gate primitives, continuous assignments, and dataflow modeling techniques with timing delays.
3	To enable students to design, simulate, and verify complex digital systems using procedural blocks, conditional execution, and control loops in behavioral modeling.
4	To impart knowledge on switch-level modeling using MOS primitives to analyze transistor-level logic behavior and timing constraints.
5	To expose students to advanced Verilog constructs, including system tasks, compiler directives, parameters, and user-defined primitives (UDPs) to build scalable, reusable design modules.

Course Content

Unit I	Introduction to Verilog HDL: Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Programming Language Interface, Module. Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space, Characters, Comments, Numbers, Strings, Logic Values, Data Types, Scalars and Vectors, Operators.
Unit II	Gate Level Modelling: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tristate Gates, Array of Instances of Primitives, Design of Flip-Flops with Gate Primitives, Gate Delay, Strengths and Contention Resolution, Net Types. Modelling at Dataflow Level: Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators.
Unit III	Behavioural Modelling: Introduction, Operations and Assignments, 'Initial' Construct, Always construct, Assignments with Delays, 'Wait' Construct, Design at Behavioural Level, Blocking and Nonblocking Assignments, The 'Case' Statement, 'If' and 'if-Else' Constructs, 'Assign- De-Assign' Constructs, 'Repeat' Construct, for loop, 'The Disable' Construct, 'While Loop', Forever Loop, sequential and Parallel Blocks.
Unit IV	Switch Level Modelling: Basic Transistor Switches, CMOS Switches, Bidirectional Gates, Time Delays with Switch Primitives, instantiation with strengths and delays, Switch level modelling for NAND, NOR and XOR.
Unit V	System Tasks, Functions and Compiler Directives: Parameters, Path Delays, Module Parameters, System Tasks and Functions, User Defined Primitives, Compiler directives. Sequential Circuit Description: Sequential Models - Feedback Model, Capacitive Model, Implicit Model.

Text Books

T.1	Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nd Edition, Pearson / Prentice Hall, 2003.
T.2	M. Morris Mano and Michael D. Ciletti, "Digital Design: With an Introduction to the Verilog HDL", 5th Edition, Pearson Education, 2012.
T.3	Zainalabedin Navabi, "Verilog Digital System Design: RT Level Synthesis, Testbench and

	Verification”, 2nd Edition, McGraw-Hill Education, 2005.
Reference Books	
R.1	Nazeih M. Botros, “HDL Programming Fundamentals: VHDL and Verilog”, Charles River Media, 2006.
R.2	Michael D. Ciletti, “Advanced Digital Design with the Verilog HDL”, 2nd Edition, Prentice Hall, 2010.
Useful Links	
1	https://onlinecourses.nptel.ac.in/noc21_ee39/preview
2	https://nptel.ac.in/courses/106105165

CO	Course Outcomes	CL	Class Sessions
CO1	Explain the fundamental concepts of Verilog HDL, its design levels, and language constructs used for hardware description.	2	9
CO2	Develop structural and dataflow models of digital circuits using gate primitives, delays, and continuous assignments.	3	9
CO3	Design and simulate digital circuits using behavioral constructs such as procedural blocks, conditional statements, and loops.	6	9
CO4	Apply switch-level primitives to model transistor-based logic circuits and analyze their timing and switch behavior.	3	9
CO5	Utilize system tasks, compiler directives, parameters, and user-defined primitives to build efficient and reusable Verilog designs.	3	9



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